THERMAL MODEL AND EXPERIMENTAL VALIDATION OF IRF 3205 MOSFET SWITCHES FOR INVERTER APPLICATION

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Abstract: Power inverters operate under dynamic loads; the varying loads cause thermal expansion and contraction, which stress the internal boundaries between the material layers in the semiconductor. Eventually, the stress wears out the semiconductor module which ultimately leads to thermally induced failure. The primary goal of this article is to present thermal model for the IRF 3205 MOSFET chip switching operation for a power inverter. The solution of the models is implemented in MATLAB R2013a environment to obtain the transient temperature profile. The transient device temperatures are recorded with a K-type thermocouple and a three channel temperature logger, MTM-380SD, with real time data logger. Results show that the experimental steady state temperatures are lower than the simulated steady state temperatures by 1.10, 1.52, 1.17 and 0.73% for pulse loads of 460W, 675W, 1015W and 1500W, respectively.

Keywords: Power inverter, IRF 3205 MOSFET, stress, thermally induced failure

Introduction

Global consumption of electricity is projected to double its 2010 value by the year 2030 (World Nuclear Association, 2010). By that time it is anticipated that nearly all electrical energy will be processed through power inverters (Krein, 2010), due to the problems associated with present day conventional sources of electrical energy generation.

One of the most controversial public debates of the last decade has addressed the effects of energy related emissions on the environment. Serious and widespread recognition and alarm have centred on air quality and, in a more global context, the greenhouse effect and the destruction of the protective ozone layer of the earth's atmosphere from CO_2 and other gases (Benemann, 1996; European Commision Community Research, 2002).

Air quality is primarily affected by SO_2 and NO_x emissions which cause acid rain and smog. A focal point of the debate has been future energy supply strategies, including the use of environmentally benign energy and conversion technologies. Key issues have been the future role of renewable energy technologies on a large scale to ensure sustainable energy growth without harmful societal impacts (Benemann, 1996; European Commision Community Research, 2002). The modern development of renewable energy technologies in the 1970's began as a result of the awareness of the finite nature of fossil fuels, specifically crude oil and natural gas.

Power inverters remain critical solar field system components, enabling electrical energy to be used more efficiently and flexibly, thereby reducing power consumption and cost. Within the power inverter, semi-conductor devices provide the means for the control and conversion of electric power by modifying voltage, current and frequency.

Problems associated with the thermal dissipation and heat transfer through power inverters is one of the most urgent issues that requires significant attention in order to produce efficient and reliable electrical energy conversion systems. The temperature dependence of semiconductor properties had been noticed and analysed since the very beginning of semiconductor research (Wilson, 1931; Wilson, 1953; Smith, 1978).

The power MOSFET is one of the most important devices for very large-scale integrated circuits and power electronics. In 1960, the MOSFET was proposed and fabricated using a thermally oxidized Silicon structure (Sze, 1980). In a MOSFET, a control signal is applied to a gate electrode that is separated from the semiconductor device surface by an intervening insulator (normally silicon dioxide). There is no significant current flow during either on state or off state in the circuit. The high input impedance is a primary feature of power MOSFETs, which greatly simplifies the gate drive circuitry (Baliga, 1987).

The possible advantage of operating MOSFETs at low temperature began to be explored in the 1970s when it became clear that higher current density and lower power loss at low temperatures would result in devices packaged in small, readily cooled volumes (Maddox, 1976; Gaensslen and Rideout, 1976). Fig. 1 shows the structure of the lateral double-diffused MOSFET (LDMOS).

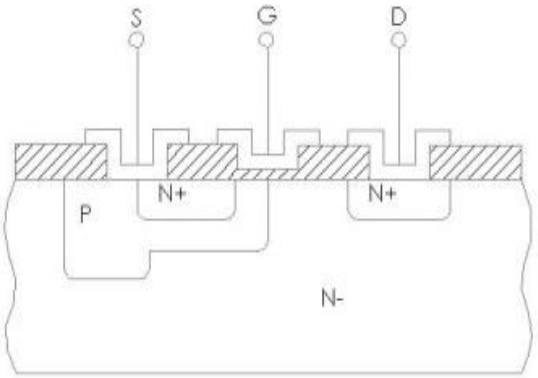

Fig. 1: Structure of the MOSFET (Sun and Plummer, 1980)

In a typical MOSFET base power inverter, power is dissipated as heat. The heat generated as a result of these losses must be conducted away from the power devices and into the environment using a heat sink. If an appropriate thermal system is not used, elevated temperatures can adversely affect electronic device operation, power handling capability, achievable packing density and crucially reliability and even risk of electrical fire outbreak. It has been showed that more than 55% of the electronic failures are caused by heat (Ericsson, 2000).

The importance of MOSFETs power module reliability has significantly increased due to widespread use of these devices in many fields, which are associated with challenging operating conditions. The reliability of a power module is of vital importance to the user, who expects the system to

operate correctly throughout its entire service life. The reliability of the whole package is tied to its temperature regime because there are many mechanisms that lead to package degradation as a result of elevated temperature and thermal cycling.

Inverters have become very important in modern technology because of the need to produce continuous supply of electrical power to critical loads such as computers, surgical equipment, security doors, automated teller machines (ATMs), telecommunications and broadcast equipment to mention but a few. Thus, inverters are in high demand and reliability in operation need be sustained.

Model Generation

There are generally two reasons to observe the IRF 3205 chip temperature used in inverter: one is the aspiration to reach smaller tolerances in the thermal design, the second is the effort to estimate the remaining power cycle lifetime of the IRF 3205 chip module. Thus, the temperature can either be measured directly or estimated by a temperature model.

Resistance – capacitance (RC) thermal model

This modeling method uses electrical RC network equivalents to represent the equivalent thermal behavior of the module, based on the use of discrete thermal components. These components are determined from the geometric and material characteristics of the module and coded as a device to be used in a circuit analysis environment, so it is coupled with the electrical circuit of the module to allow for the simulation of a complete electro-thermal model.

There are two common types of RC network models: the Foster and the Cauer network, although both networks are used to represent the resistance and capacitance values of the structures, their topologies and construction are different which reflects in different resistance and capacitance values, as shown diagrammatically in Fig. 2.

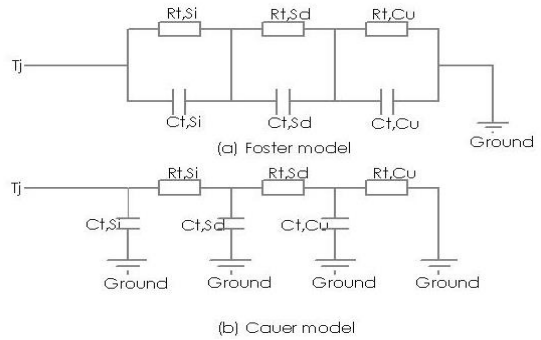

Fig. 2(a,b): RC network models

Cauer network model

Cauer network model can be developed based on the physical geometry of the IRF 3205 MOSFET switch (dimensions and material properties). The Cauer network is based on the physical structure of the system with every capacitor connected to the ground as shown in Fig. 2(b). Each resistance value represents the thermal resistance between adjacent nodes and each capacitance values the mass at a node.

However, a single equation for the junction temperature, $T_{j\text{-}c}(t)$ cannot be modelled and the thermal resistance and capacitance can be transformed to Foster network model.

Foster network model

Foster RC network model has the configuration consisting of parallel resistance and capacitance sub circuits connected in series as shown in Fig. 2(a). The product of each RC set in the network provides a time constant, τ, which is the time taken for the temperature at the constant heat flux surface to be affected by the geometry at a thickness, d, from the surface. The time constant is used to calculate the time it takes for the heat to fully penetrate a layer of thickness. This is very useful as it is possible to calculate the time during which a heat pulse that each layer in the IFR 3205 MOSEFET stack up becomes influential in the device temperature.

These time constants are combined to form a single equation for the junction temperature, Tj-c(t) for the IRF 3205 MOSFET chip. However, the challenge is that the time constants for this model are typically found by fitting a curve, to the measured transient thermal response from an experimental method, where the time constants are extracted from the equation for the fitted curve. However, the objective of this research is to model the thermal response from the geometrical structure and material properties of the IRF 3205 MOSFET switch.

Thermal model

The junction temperature in a first-order circuit can be estimated with an equivalent electronic RC circuit with a current source. The electric current corresponds to the power loss, the voltage across the resistor corresponds to the temperature difference, the electrical capacitance, C, to the thermal capacitance, C_t, and the electrical resistance, R, to the thermal resistance, R_t. Fig. 3 shows the electrical to thermal transformation.

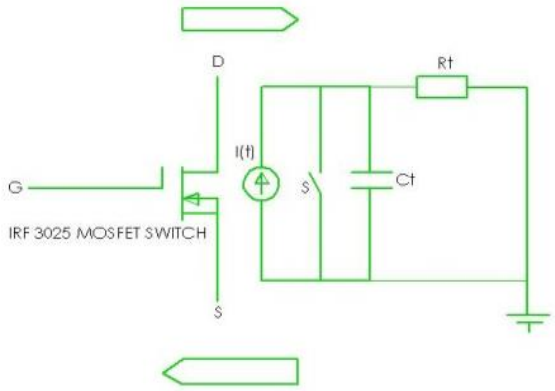

Fig. 3: Principle of electro-thermal modeling

The power loss model forms the input required for the thermal model and is the average power dissipated by the semiconductor devices in the power inverter. The solution to the thermal model is only made possible with power loss data from a power loss model. The power losses of the IRF 3205 MOSFET chip are divided into the static power losses and the non-static power losses. The static power losses are the on-state losses (conduction losses) and the blocking losses. The non-static losses are divided into the switching losses (on/off) and driving losses, the type of losses in the inverter depends on the switching frequency. However, the blocking losses and driving losses are normally small and are negligible (Rajapakse *et al*, 2005):

Thus;

$$P_L = P_c + P_{sw} \quad (1)$$

Where: P_c is the conduction loss, W, P_{sw} is the switching loss, W. The conduction losses in IRF 3205 MOSFET chip can be calculated using a MOSFET approximation with the drain-source on state resistance (R_{DSon}),

$$P_{CM} = R_{DSon} \times I_{Drms}^2 \quad (2)$$

I_{Drms} is the rms value of the IRF 3205 MOSFET on state. The typical R_{DSon} can be taken from the datasheet of IRF 3205 MOSFET manufacturer.

Switching loss originates during the device transition from the on state to the off state and vice-versa (Jauregul *et al.*, 2011). When a semiconductor component is turned on, the device aims to switch from the blocking state to an unblocking state. The turn on energy losses in power IRF 3205 MOSFET (EonM) can be calculated as presented by Rajapakse *et al.* (2005) and Weinberg (1962):

$$E_{onM} = U_{DD} \times I_{Don} \times \frac{t_{ri}+t_{fu}}{2} + Q_{rr} \times U_{DD} \quad (3)$$

Where: tri is the current rise time, tfu is the voltage fall time, I_{Don} is the drain current, UDD is the Inverter supply voltage (DC), Q_{rr} is the reverse recovery charge.

The switch off energy losses can similarly be obtained as:

$$E_{offM} = U_{DD} \times I_{Doff} \times \frac{t_{ru}+t_{fi}}{2} \quad (4)$$

Where: t_{ru} is the voltage rise time, t_{fi} is the current fall time.

The switching losses in the IRF 3205 MOSFET chip are the product of switching energies and the switching frequency:

$$P_{swM} = (E_{onD} + E_{offM})f_{sw} \quad (5)$$

Carrying out loss balance, power losses in the IRF 3025 MOSFET can be expressed as the sum of the conduction and switching losses giving:

$$P_M = P_{CM} + P_{swM} = R_{DSon} \times I_{Drms}^2 + (E_{onM} + E_{offM})f_{sw} \quad (6)$$

The power dissipated is a function of the duty ratio, equation (6) can be expressed as:

$$P_d = \Delta t_{on} f_{sw}\left(R_{DSon} \times I_{Drms}^2 + (E_{onM} + E_{offM})f_{sw}\right) \quad (7)$$

From equation (3) and equation (4), the power dissipated is obtained as:

$$P_d = (\Delta t_{on} f_{sw})\left[\left(R_{DSon} \times I_{Drms}^2\right) + \left(U_{DD} \times I_{Don} \times \frac{t_{ri}+t_{fu}}{2} + Q_{rr} \times U_{DD} + U_{DD} \times I_{Doff} \times \frac{t_{ru}+t_{fi}}{2}\right) f_{sw}\right] \quad (8)$$

The step response of the circuit of figure 3 can be analyzed by current equations. The voltage U=U(t) for any given time time, t, is:

$$U(t) = RI\left(1 - e^{-\frac{t}{RC}}\right) \quad (9)$$

Using the current-power analogy and denoting RC as τ, the temperature difference, Tj-c(t) for the IRF 3205 MOSFET chip for the power inverter is obtained as:

$$T_{j-c}(t) = R_t P_d\left(1 - e^{-t/\tau}\right) \quad (10)$$

For the three layers structure of the IRF 3205 MOSFET chip is:

$$T_{j-c}(t) = P_d \sum_{i=1}^{n} R_{ti}\left(1 - e^{-t/\tau_i}\right) \quad (11)$$

From equation (8), the transient thermal model is:

$$T_{j-c}(t) = (\Delta t_{on} f_{sw})\left[\left(R_{DSon} \times I_{Drms}^2\right) + \left(U_{DD} \times I_{Don} \times \frac{t_{ri}+t_{fu}}{2} + Q_{rr} \times U_{DD} + U_{DD} \times I_{Doff} \times \frac{t_{ru}+t_{fi}}{2}\right) f_{sw}\right]\left(\sum_{i=1}^{n} R_{ti}\left(1 - e^{-t/\tau_i}\right)\right) \quad (12)$$

Table 1 shows the material properties and physical dimension of IRF 3205 MOSFET used for simulation.

Table 1: Properties and dimension of IRF 3205 MOSFET chip for computations

Layer	Material	k (W/mK)	ρ (kg/m3)	Cp (J/kgK)	L (m)	W (m)	D (m)
Die	Silicon	150	2330	710	0.007	0.009	0.00042
Solder	95PbSn	32.3	11000	134	0.007	0.009	0.0001
Base-plate	Copper	386	8954	380	0.018	0.014	0.002

The Foster network is the preferred network for the thermal simulations, this model tends to be concerned with the junction temperature on which the reliability of the power inverter lies and can be calculated once the time constants have been extracted.

Cauer to Foster transformation

The method that is used to synthesize the network is called Continuous Fraction Expansion. The transformation algorithm is based on the expression of the RC components in the frequency domain. Using Fig. 4, the time dependent thermal dissipation of the Cauer circuit can be expressed as:

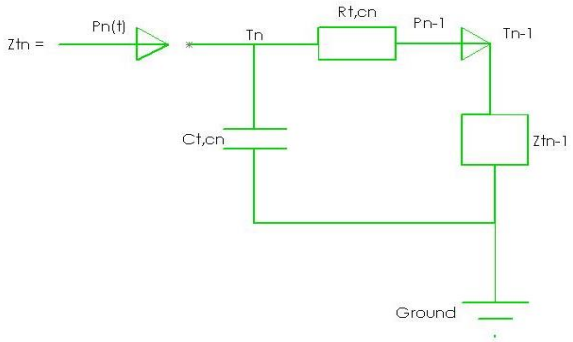

Fig. 4: Recursive Cauer circuit diagram

$$P_n(t) = P_{n-1}(t) + C_{t,cn}\frac{d}{dt}T_n(t) \quad (13)$$

$$P_{n-1}(t) = \frac{T_n(t) - T_{n-1}(t)}{R_{t,cn}} \quad (14)$$

And the convolution integrals of the Cauer circuit can be expressed as:

$$T_n(t) = \int_0^t P_n(\tau) Z_t C_{t,cn}(t-\tau)d\tau \quad (15)$$

$$T_{n-1}(t) = \int_0^t P_{n-1}(\tau) Z_t C_{t,c(n-1)}(t-\tau)d\tau \quad (16)$$

Equation (13), equation (14), equation (15) and equation (16) are transform to algebraic system using Laplace transformation. Laplace transformation of equation (13) and equation (14) yields:

$$P_n(s) = P_{n-1}(s) + C_{t,cn} s T_n(s) \quad (17)$$

$$P_{n-1}(s) = \frac{T_n(s) - T_{n-1}(s)}{R_{t,cn}} \quad (18)$$

The Laplace transformation of equation (15) and equation (16) yields:

$$T_n(s) = P_n(s) Z_t C_{t,cn}(s) \quad (19)$$

$$T_{n-1}(s) = P_{n-1}(s) Z_t C_{t,c(n-1)}(s) \quad (20)$$

The thermal impedance of the Cauer circuit is defined as:

$$Z_t(s) = \frac{T_n(s)}{P_n(s)} \quad (21)$$

Substituting equation (17) and equation (19) into equation (21), The recursive definition of the thermal impedance of the Cauer circuit can then be expressed as:

$$Z_t = \frac{1}{sC_{t,cn} + \frac{1}{R_{t,cn} + \frac{1}{sC_{t,c(n-1)} + \cdots + \frac{1}{R_{t,1}}}}} \quad (22)$$

Equation (22) is a continued fraction representation, which can be expressed as a rational fraction in s as:

$$Z_t = \frac{N_2 s^2 + N_1 s + N_0}{D_3 s^3 + D_2 s^2 + D_1 s + D_0} \quad (23)$$

Where s is the Laplace variable and the numerator coefficients are:

$$N_2 = C_{t,c2} \times C_{t,c3} \times R_{t,c1} \times R_{t,c2} \times R_{t,c3} \quad (24)$$

$$N_1 = C_{t,c2}R_{t,c1}R_{t,c2} + C_{t,c2}R_{t,c1}R_{t,c3} + C_{t,c3}R_{t,c3}R_{t,c1} + C_{t,c3}R_{t,c3}R_{t,c2} \quad (25)$$

$$N_0 = R_{t,c2} + R_{t,c1} + R_{t,c3} \quad (26)$$

Denominator coefficients are:

$$D_3 = C_{t,c1}C_{t,c2}C_{t,c3}R_{t,c1}R_{t,c2}R_{t,c3} \quad (27)$$

$$D_2 = C_{t,c1}C_{t,c2}R_{t,c1}R_{t,c2} + C_{t,c1}C_{t,c2}R_{t,c1}R_{t,c3} + C_{t,c1}C_{t,c3}R_{t,c1}R_{t,c3} + C_{t,c1}C_{t,c2}R_{t,c2}R_{t,c3} + C_{t,c2}C_{t,c3}R_{t,c2}R_{t,c3} \quad (28)$$

$$D_1 = C_{t,c1}R_{t,c1} + C_{t,c2}R_{t,c2} + C_{t,c1}R_{t,c3} + C_{t,c2}R_{t,c2} + C_{t,c2}R_{t,c3} + C_{t,c3}R_{t,c3} \quad (29)$$

$$D_0 = 1 \quad (30)$$

Equation (13) is resolved into partial fraction of the form:

$$Z(s) = \frac{A_1}{s-s_1} + \frac{A_2}{s-s_2} + \frac{A_3}{s-s_3} \quad (31)$$

s_1, s_2, s_3, A_1, A_2 and A_3 are numerical values. The Foster impedance thermal parameters are readily extracted from equation (31).

Experimental setup

A prototype test system is designed and fabricated to verify the thermal model. The setup allows the measurement of the IRF3205 MOSFET chip temperature for varying inverter load conditions. The experimental set up consists of the inverter, Clamp meter, Multimeter, MTM–380SD 3 Channels Temperature Monitor with SD Card Datalogger, the battery bank and solar fields. The MTM–380SD 3 Channels Temperature Monitor with SD Card Datalogger was used to monitor the chip temperature, while the AC output voltage and current and DC input voltage and current are measured with the aid of the Clamp meter and multimeter. The input voltage to the power inverter was created from a battery bank fully charged by the solar field. Figure 5 shows the picture of the battery bank.

Fig. 5: Battery Bank

While Fig. 6 shows the solar field array.

Fig. 6: Solar field array

Figure 7 shows the power inverter during a test run.

Fig. 7: Prototype inverter setup

The inverter was pulsed with a series of different power levels and temperature measurements were made with the aid of MTM–380SD 3 Channels Temperature Monitor with SD Card Datalogger. The active time for each inverter power level is long enough for the inverter and thermal network being validated to reach a steady state condition.

The device under test is a 24 VDC copper base plate transfer molded power IRF3205 MOSFETs chip in TO 220AB case, with chip size of approximately 9 x 7 mm. Top side of the power semi conductor chip is wire bonded while the bottom side is soldered on copper lead frame of 2 mm thickness which provides heat transfer path into the heat sink. The package is moulded with resin to fix the leads for external electrical connections; this technology provides low operating costs, however, the required external isolation between circuit and heat sink increases mounting effort.

Experimental results are presented in the form of transient device temperature, which are recorded with the aid of MTM–380SD 3 Channels Temperature Monitor with SD Card Datalogger. Fig. 8 shows the photograph of the MTM-380SD K-Type thermocouple temperature datalogger.

Fig. 8 MTM-380SD K-Type thermocouple temperature datalogger

Results and Discussion

Simulated and experimental plots at various load conditions

Figure 9 compares result generated by the thermal model and experimental data for an inverter load condition of 460W, 675W, 1015W, and 1500W respectively. The result of the simulation is that of a 24VDC/2.5K.V.A voltage source inverter using PWM at 50Hz frequency at an output voltage of 220VAC.

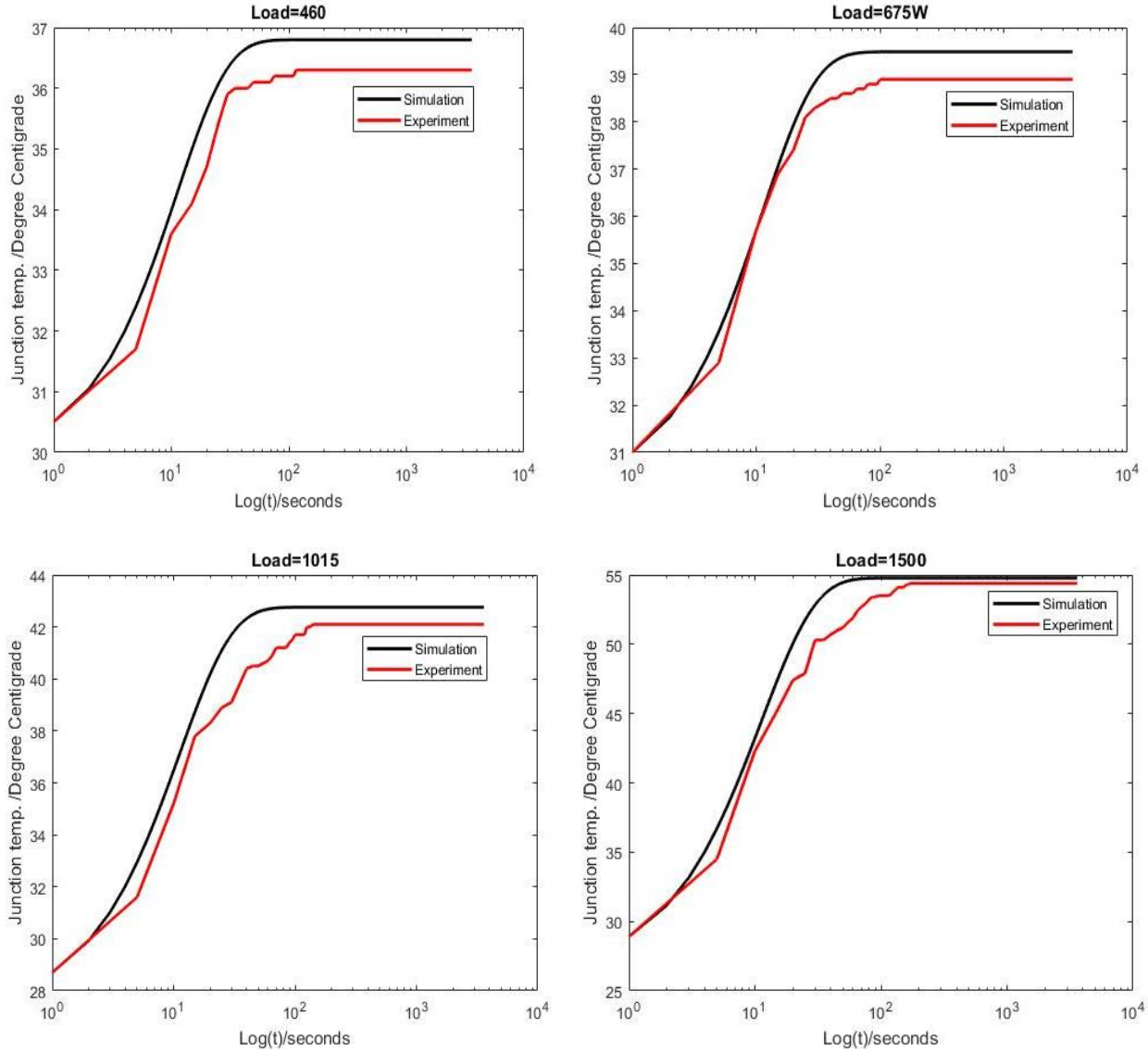

Fig. 9: Thermal model simulation and experimental plots

The transient device temperatures simulated by the thermal model match the results captured by the Lutron MTM-380 SD temperature data logger closely over the duration of the loading condition. The result of the simulation and experimental plot show an exponential build up function with a rising temperature profile that increases with time until steady state condition.

However, the thermal model attain steady state equilibrium temperature of about 36.7ºC in about 80s while experimental data attain steady state condition temperature of 36.3ºC at 115s, implying 1.1% deviation in steady state temperature for the 460W load condition, the thermal model attain steady state equilibrium temperature of about 39.5ºC in about 75s while experimental data attain steady state condition temperature of 38.9ºC at 105s, implying 1.5% deviation in steady state temperature for the 675W load condition.

The thermal model attain steady state equilibrium temperature of about 42.6ºC in about 70s while experimental data attain steady state condition temperature of 42.1ºC at 140s, implying 1.2% deviation in steady state temperature for the 1015W load condition, the thermal model attain steady state equilibrium temperature of about 54.8ºC in about 80s while experimental data attain steady state condition temperature of 54.4ºC in 170s, implying 0.7% deviation in steady state temperature, for the 1500W load condition. The slight deviation between the simulated and experimental results could be attributed to the effect of the glue on the thermocouple probe.

Conclusion

Power inverters are essentially for supplying energy for today's society in a more efficient, sustainable and controllable manner. Thermally induced failures modes are the main causes of power inverter reliability issues. Thus, a resistance – capacitance (RC) thermal models was created which has the capability of representing the thermal behaviour of the power inverter.

The created RC thermal model employs the Foster network as the basic circuit configuration that can effectively predict the junction temperature during the ON/OFF switching of the IRF3205 MOSFET chip on which the reliability of the whole power inverter depends according to Arrhenius reliability model.

The thermal model simulation shows that transient device temperatures profile is an exponential build up function, increasing rapidly during the switching operation until steady state is attained. Results show that the experimental steady state temperatures are lower than the simulated steady state temperatures by 1.10%, 1.52%, 1.17% and 0.73% for pulse loads of 460W, 675W, 1015W and 1500W, respectively.

The Foster thermal model developed is a useful early design tool since it allows various packaging geometries and materials to be investigated efficiently, as the results generated by the thermal model are very realistic, and provides a useful guidance in all test cases for a power inverter design engineer. Also, a single equation for the junction temperature which the packaging materials reliability depend is modeled which is a simpler approach compared to other methods that employ curve fitting, where time constants are extracted from the equation of fitted curve obtained from experimental data.

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